Stepenko, S.; Husev, O.; Vinnikov, D.; Ivanets, S., "FPGA control of the neutral point clamped quasi-Z-source inverter," in 2012 13th Biennial Baltic Electronics Conference (BEC), pp.263-266, 3-5 Oct. 2012. doi: 10.1109/BEC.2012.6376867

This paper is a previously accepted version of the article.
The final published version is available in IEEE Xplore Digital Library
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6376867&isnumber=6376805

Даний матеріал є версією статті, прийнятої до публікації.
Кінцева опублікована версія статті доступна в електронній бібліотеці IEEE Xplore
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6376867&isnumber=6376805

FPGA Control of the Neutral Point Clamped Quasi-Z-Source Inverter

S. Stepenko[1,2], O. Husev[1,2], D. Vinnikov[1], S. Ivanets[2]

[1]*Department of Electrical Drives and Power Electronics, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia, E-mail: dmitri.vinnikov@gmail.com*
[2]*Department of Industrial Electronics, Chernihiv State Technological University, Shevchenko street 95, 14027 Chernihiv, Ukraine, E-mail: stepenko.sergey@gmail.com*

ABSTRACT: The three-level neutral point clamped quasi-Z-source inverter has been proposed recently. Due to its features the neutral point clamped quasi-Z-source inverter is especially suitable for renewable energy sources. This topology requires special control methods and respectively new element basis can be used for control implementation. Current paper describes the control system implemented, based on FPGA for a three-level neutral point clamped quasi-Z-source inverter and the control signals obtained.
KEYWORDS: FPGA, control system, three-level inverter, neutral point clamped inverter, quasi-Z-source inverter.

1 Introduction

A new modification of the quasi-Z-source inverter, a three-level neutral point clamped quasi-Z-source inverter, has been proposed recently [1]. Its topology is shown in Fig. 1.

This topology is a combination of the quasi-Z-source inverter (qZSI) and the three-level neutral point clamped inverter (3L-NPC). The new converter comprises advantages of both of these topologies: it can buck and boost the input voltage, it has excellent short circuit immunity and due to the multilevel topology, high energy density is attainable [2].

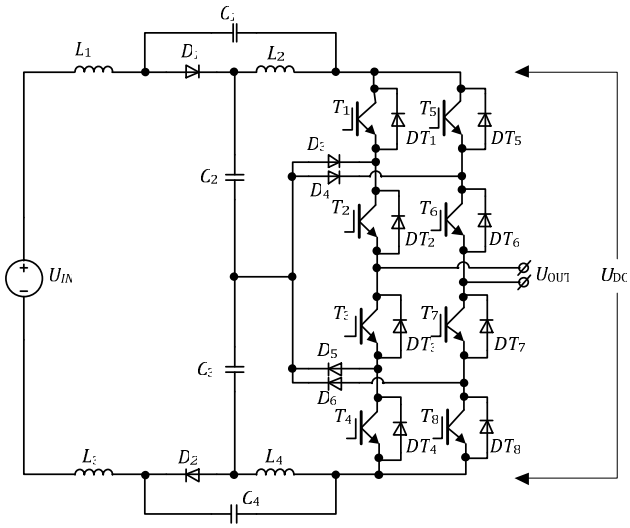

Fig. 1. Neutral point clamped quasi-Z-source inverter

Each leg of the neutral point clamped quasi-Z-source inverter consists of two complementary switching pairs of transistors and four anti-parallel diodes (Fig. 1).

This topology has also such advantages as continuous input current, the possibility to use shoot-through, lower switching and balanced neutral-point voltage losses in comparison with the traditional two-level voltage source inverter [1]. Due to the above features the neutral point clamped quasi-Z-source inverter is especially suitable for renewable energy sources.

To manage the 3L-NPC qZSI eight control signals applied to the gates of power switches (e.g. MOSFETs, IGBTs) and a shoot-through separately formed signal are required. Finally, the generated shoot-through vector will be mixed with other control signals. These signals should be shifted and have different shape. To satisfy such requirements using microcontroller will be quite difficullt and therefore new element base for control is necessary.

2 Basis for Control Implementation

In recent years implementations based on Field Programmable Gate Arrays (FPGAs) have become common in different areas of electronics.

There are many studies devoted to embedded systems (Systems-On-Chip) that cover the main problems of their usage, both in the industry and academia. Accordingly, each year at the most prestigious conferences numerous papers describing the newest features of FPGAs have been reported. For example, in some cases if we need, it is possible now to emulate large systems that cannot even be placed into existing FPGA [3]. In turn, the possibilities of FPGAs (due to their advantages, such as fast prototyping, reprogramming, high operating frequency, and parallel processing capabilities) are increasingly used in power electronics to control the DC/AC converters (inverters) in order to achieve the desired output voltage. The implementation of control for various types of voltage source inverters (VSI) using FPGA was proposed in [4], [5] and several practical examples of its application demonstrate the utility of such approaches.

In addition to the above features of FPGAs, there is also the possibility to use the Nios II embedded processor, which can be built by a designer through a software [6].

The digital Sinusoidal Pulse Width Modulation (SPWM), typically based on microcontrollers (MCUs), Digital Signal Processors (DSPs) or FPGAs, is commonly used to realize the control algorithms of the DC/AC inverters [7].

Many researchers have chosen to implement PWM by DSP or MCU. This approach has the advantages of simple circuitry, software realization and flexibility. However, there are also several disadvantages [5]:

• If the DSP or MCU is not able to provide enough on-chip peripherals, such as comparators and dead-time controllers to support the PWM outputs, extra hardware circuits need to be designed to cooperate with the controller.

• As the levels of the inverter increase and the inverter structure becomes more complex, the programming of the corresponding PWM in the DSP or MCU becomes one of the most time-consuming tasks.

Accordingly, when dealing with the implementation of the control system for a multi-level inverter, as a rule, FPGAs are used. The FPGA-based control systems for a 3-level inverter are described in [8], [9], [10] and for a 5-level inverter in [5], [11].

However, despite the wide opportunities of the FPGAs, some developments to manage the converters are performed using with FPGA an additional microcontroller [8] or a digital signal processor [5], [9] to calculate the reference voltages.

There are many studies where the control system based on FPGA is used to control NPC inverters [9], [10], [12]. In [13] it was proposed to use FPGA in order to control a Z-Source inverter for a wind energy conversion system, although no corresponding experimental results have been presented.

Currently no studies are available that deal with building a control system based on FPGA to manage a 3L-NPC qZSI, because this topology has been proposed quite recently.

In this paper the control system based on FPGA for a 3L-NPC qZSI will be described and the obtained control signals will be presented. In addition to the above advantages, the use of FPGA makes it easier to implement a shoot-through mode that is important for the given topology [1].

There are numerous FPGAs families available to choose from different vendors. In some designs to manage the power converters the FPGAs of Stratix [4] or Cyclone [6] families from Altera Corporation were used. In other designs the FPGAs of Virtex [7] or Spartan [11] families from Xilinx Corporation were used.

Table 1 shows the comparison of the performance of DSP applications in Altera FPGAs with DSP processors as well as competitive FPGA offerings. In addition, the detailed performance data for Cyclone II and Spartan-3 FPGAs is presented in [14]. Altera's low-cost Cyclone II FPGAs offer up to 2 times higher performance and an average of 1.5 times higher performance than the Xilinx Spartan-3 family.

TABLE 1

ADVANTAGES OF ALTERA DSP PERFORMANCE

Comparison Category	Altera Performance Advantage
Altera FPGAs vs. DSP processors	10x DSP processing power per dollar
High-performance FPGAs comparison: Altera's Stratix II FPGAs vs. Xilinx's Virtex-4 FPGAs	Up to 1.8x and on-average 1.2x higher performance
Low-cost FPGAs: Altera's Cyclone II FPGAs vs. Xilinx's Spartan-3 FPGAs	Up to 2x and on-average 1.5x higher performance

Based on the benchmarked data [14], the Cyclone II device family operated at over 200 MHz in 9 of the 17 designs and one FIR design exceeded 300 MHz. None of the 17 designs in Spartan-3 devices operated above 200 MHz. In addition, Cyclone II FPGAs outperform Spartan-3 devices in all designs benchmarked. This performance advantage can directly translate to higher channel count or lower cost for typical designs.

3 System Description

Fig. 2 illustrates the proposed functional structure of the system. The direction of control is shown by the arrows.

In the current work the above control system for the 3L-NPC qZSI was built based on the FPGA Cyclone II EP2C5T144C8 from Altera [15]. In order to implement the control algorithm the VHDL was used. VHDL is a VHSIC (Very High Speed Integrated Circuits) Hardware Description Language.

The control system, in addition to FPGA, also contains Matching Board and Driver Board. An optical connection between the Matching and Driver Boards has been provided. In this way, the system can be managed as far as it is limited by the length of fiber. The Driver Board contains eight channels each of them consisting of receivers (HFBR-2528Z), driver ICs (ACPL-H312) and necessary passive components. The drivers are directly controling the MOSFETs of the NPC-qZSI. The output voltage from the NPC-qZSI is connected to the power grid through the output filter.

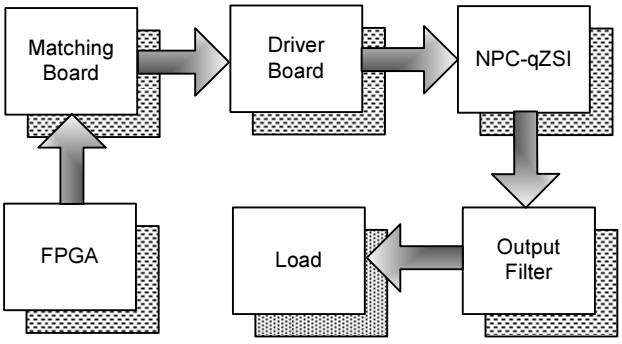

Fig. 2. The structure of the system

The principle of building the control signals through FPGA using a special modulation technique is shown in Fig. 3.

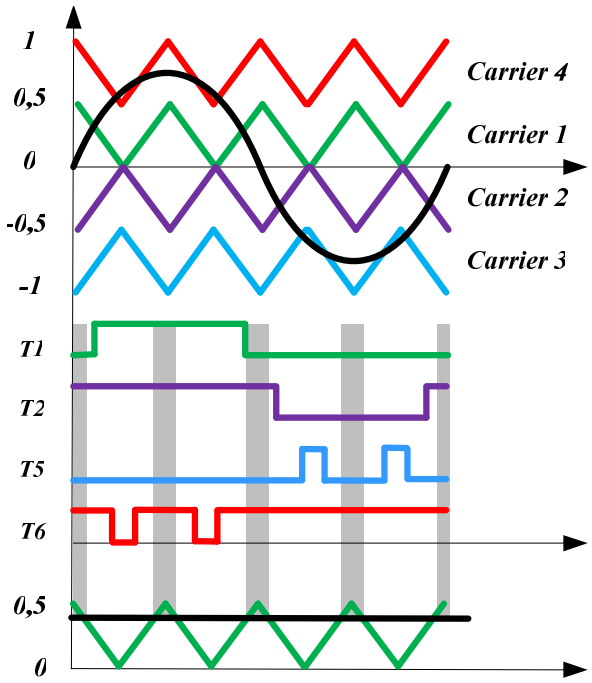

Fig. 3. The sketch of the proposed modulation technique

One modulating sinusoidal wave and four triangular carriers (*Carrier 1– Carrier 4*) are compared in order to obtain required states of the switches T1, T2, T5, T6 and switches T3, T4, T7, T8 have the complementary states, respectively (Fig. 1).

Carrier 1 is used also to generate the shoot-through states being compared with a constant that includes the desired value of the shoot-through duty cycle. Operating in this way, uniformly distributed shoot-through states with constant width during all the output voltage period can be achieved.

The abovementioned modulation technique has been developed in order to provide the necessary quality of the output voltage with gain capabilty [2].

4 Experimental results

The results of the experimental investigations of the control system have proved suggested work of the FPGA-based control system to be applicable for the NPC qZSI.

The signals applied to the gates of the power converter switches (MOSFETs were used) in the case without the shoot-through state are shown in Fig. 4.

The signals applied to the gates of the power converter switches in the case when the shoot-through state was used are shown in Fig. 5. The shoot-through states are distributed during whole low-level time of gate voltages.

In both of the figures only the gate signals of the switches T1, T2, T5, T6 have been presented because the above switches have the complementary state with T3, T4, T7, T8 respectively.

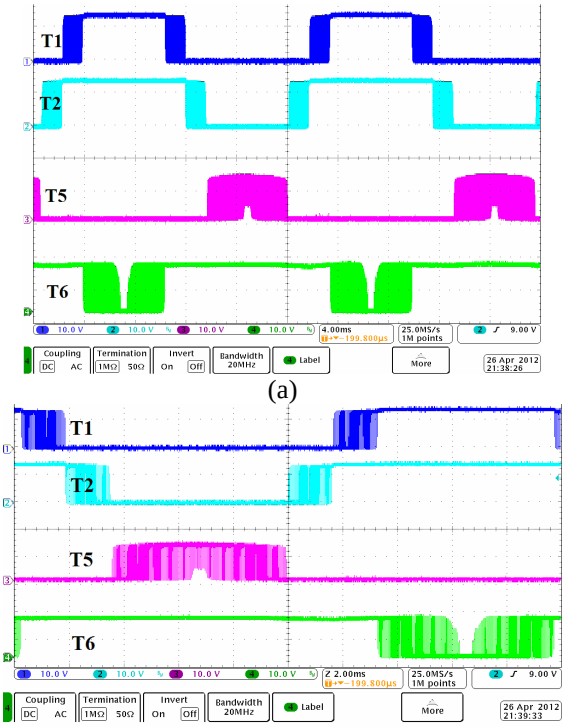

Fig. 4. The control signals applied to the gates of switches without the shoot-through state (a) and scaling (b)

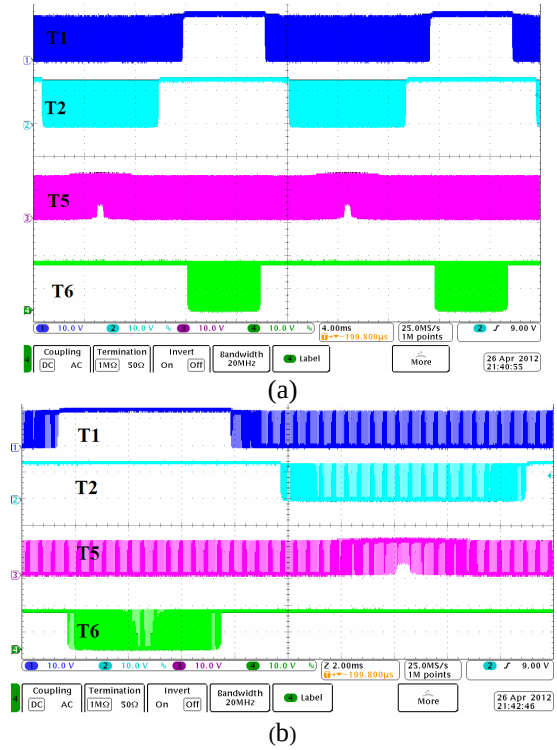

Fig. 5. The control signals applied to the gates of the switches with the shoot-through state (a) and scaling (b)

The amplitude of signals formed by control system and applied to the gates of power switches is 12 V. The modulation frequency of the control system is 25 kHz. It is also evident that the load per each MOSFET is different and the most loaded switch is T5. The frequency of the output voltage formed by 3L-NPC qZSI is 50 Hz.

As can be seen the control system forms necessary shape of voltage for each gate. Four control signals for the gates of MOSFETs T1, T2, T5, T6 have different duty cycles and shifting. Therefore such required signals can't be obtained using microcontroller's PWM, but it have been done using FPGA.

5 Conclusion

In this study the implemented control system based on the FPGA Cyclone II EP2C5T144C8 using a special modulation technique for a three-level neutral point clamped quasi-Z-source inverter has been described and the obtained control signals for power switches have been presented. The results of the experimental investigations with as well as without shoot-through states have proved the suggested work of the FPGA-based control system to be applicable for 3L-NPC qZSI.

Acknowledgment

Authors wish to thank for their support Estonian Ministry of Education and Research (Project SF0140016s11), Estonian Science Foundation (Grants ETF8538 and ETF8687) and Estonian Archimedes Foundation (Project "Doctoral School of Energy and Geotechnology II").

Also, authors are grateful to the Rector of Tallinn University of Technology Andres Keevallik and to the Rector of Chernihiv State Technological University Serhiy Shkarlet for the development of the international scientific cooperation between these two universities.

References

[1] S.Ott, I.Roasto, D.Vinnikov, "Neutral point clamped quasi-impedance-source inverter". 7th International Conference-Workshop Compatibility and Power Electronics (CPE'11, Tallinn, Estonia, June 2011), pp.348-353.

[2] S.Ott, I.Roasto, D.Vinnikov, T.Lehtla, "Analytical and Experimental Investigation of Neutral Point Clamped Quasi-Impedance-Source Inverter". Scientific Journal of RTU, series.4, Enerģētika un elektrotehnika, vol.29, pp.113-118, 2011.

[3] U.Reinsalu, A.Arhipov, P.Ellervee, "Architectural exploration tasks for on-chip embedded systems". 11th International Biennial Baltic Electronics Conference (BEC'08, Tallinn, Estonia, Oct. 2008), pp.171-174.

[4] D.Puyal, L.A.Barragan, J.Acero, J.M.Burdio, I.Millan, "An FPGA-Based Digital Modulator for Full- or Half-Bridge Inverter Control". IEEE Transactions on Power Electronics, vol.21, no.5, pp.1479-1483, 2006.

[5] D.Ning-Yi, W.Man-Chung, N.Fan, H.Ying-Duo, "A FPGA-Based Generalized Pulse Width Modulator for Three-Leg Center-Split and Four-Leg Voltage Source Inverters". IEEE Transactions on Power Electronics, vol.23, no.3, pp.1472-1484, 2008.

[6] J.Liu, M.Liao, W.Chen, D.Xu, "Research on inverter based on Nios II and system design". 4th IEEE Conference on Industrial Electronics and Applications (ICIEA'09, Xi'an, China, May 2009), pp.1441-1446.

[7] M.Lakka, E.Koutroulis, A.Dollas, "Design of a High Switching Frequency FPGA-Based SPWM Generator for DC/AC Inverters". International Conference on Field Programmable Logic and Applications (FPL'11, Chania, Greece, Sept. 2011), pp.15-19.

[8] L.H.S.C.Barreto, P.P.Praca, C.M.T.Cruz, R.T.Bascope, "PID Digital Control Using Microcontroller and FPGA Applied to a Single-Phase Three-Level Inverter". 22nd Annual IEEE Applied Power Electronics Conference (APEC'07, Anaheim, California, USA, Feb-March 2007), pp.1443-1446.

[9] J.Liu, Z.Zhang, X.Yin, M.Wen, "FPGA Implementation of a Multi-Level SPWM for Three-Level NPC Inverter". 41st International Universities Power Engineering Conference (UPEC'06, Newcastle upon Tyne, UK, Sept. 2006), pp.175-179.

[10] R.Stala, "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs". IEEE Transactions on Industrial Electronics, vol.58, no.9, pp.4185-4195, 2011.

[11] P.Palanivel, S.S.Dash, "A FPGA based Variable switching frequency Multi-carrier Pulse width modulation for Three phase Multilevel Inverter". International Conference on Control, Automation, Communication and Energy Conservation (INCACEC'09, Perundurai, Tamilnadu, India, June 2009), pp.1-4.

[12] O.Lopez, J.Alvarez, J.Doval-Gandoy, F.D.Freijedo, A.Nogueiras, A.Lago, C.M.Penalver, "Comparison of the FPGA Implementation of Two Multilevel Space Vector PWM Algorithms". IEEE Transactions on Industrial Electronics, vol.55, no.4, pp.1537-1547, 2008.

[13] R.Bharanikumar, R.Senthilkumar, A.C.Yazhini, A.N.Kumar, "FPGA Controller Based Z-Source Inverter for Wind Turbine Driven Permanent Magnet Generator". Joint International Conference on Power System Technology and IEEE Power India Conference (POWERCON'08, New Delhi, India, Oct. 2008), pp.1-5.

[14] FPGAs for High-Performance DSP Applications. White Paper. Altera Corporation, 2005.

[15] Cyclone II Device Handbook, Volume 1. Altera Corporation, 2007.